Md Imran Momtaz

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PhD student | School of Electrical and Electronic Engineering | Georgia Institute of Technology

OBJECTIVE

A highly energetic individual actively looking for fulltime opportunity in the fields of electronic system design, verification, and testing. 2+ years of experience in detection, diagnosis, and correction of different faults of autonomous systems and analog and mixed signal circuits and systems.

EDUCATION

PhD in Electrical and Computer Engineering **Current GPA: 3.86/4.00** — Fall 2014 – Present
Georgia Institute of Technology, Atlanta, GA **(Expected graduation: May, 2019)**

M.Sc. in Electrical and Electronic Engineering **CGPA: 3.83/4.00** — Nov 2009 – Oct 2011
Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh

B.Sc. in Electrical and Electronic Engineering **CGPA: 3.92/4.00, Rank: 4/138 (In Dept. of EEE)** — Dec 2004 – Oct 2009
Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh

SKILLS POSSESED

COMPUTER SKILLS

- Machine learning tool: Keras, Tensorflow
- Circuit Simulation Tools: Hspice, Orcad, Quartus, Cadance, LTSpice, ADS, SIMPLIS
- Programming Languages : C/C++, MATLab, Python, Shell scripting
- O/S : Windows 7/8.1/10, MS DOS, Ubuntu
- Typesetting Software: LaTex

PROFESSIONAL EXPERIENCES

Graduate Research Assistant, Low Power Adaptive and Resilience Laboratory, Georgia Institute of Technology — Fall 2015 - Present

1. Working on error detection, diagnosis, and correction of autonomous system in real time.
2. Working on error detection, and diagnosis of electronic circuits from pre-Silicon to post-Silicon validation.

Graduate Technical Intern at Intel Corporation — Fall 2017
Worked on simulator performance enhancement. Implemented pruning tool for circuit netlist to remove unnecessary part of the netlist. Was able to reduce simulation run-time.

Verification Engineering Intern at Texas Instruments — Summer 2017

a) Created a tool which automates the flow from verification plan to verification simulation. The tool has been applied to power converters. It automates the whole process from plan to simulation without human help and saves working time for this.

b) Created a tool which updates the verification checkers automatically from specification. The tool incorporates the specifications from central system and updates the checkers from there saving human hours.

Design Engineering Intern at Texas Instruments — Summer 2016
Created a tool from scratch which automates the flow of product from architecture to IC. The tool has been applied to power converters. It automates the whole process of creating the circuit in another environment, verifies the same automatically and saves working time for this.

Graduate Teaching Assistant, School of ECE, Georgia Institute of Technology. — Fall 2014 – Summer 2015
Set the questions, graded the scripts for ECE 2020 and ECE 3741. Helped about 260 students.

Assistant Professor, Department of EEE, BUET, Dhaka — Jun 2013 – Aug 2014
Conducted undergraduate class of 120 students on basic electronic circuits and systems. Completed official duties assigned.

Lecturer, Department of EEE, BUET, Dhaka — Jan 2010 – Jun 2013
Conducted undergraduate class of 300 students on basic electronic circuits and systems and energy conversion. Completed official duties assigned.

Research/Project:

1. 4 tap FIR filter: A complete digital logic cell library was implemented in Cadence Design Systems environment and a 4 tap digital FIR filter has been implemented using this library. Verified the design with DRC and LVS check.
2. Study of power leakage at sub 45 nm system: Different techniques to reduce leakage power consumption of deep sub-micron circuits were studied. Implemented in Cadence Design Systems environment.
3. Concurrent error detection of autonomous system: Concurrent error detection circuits of a state variable system was implemented in MATLAB. Errors were injected and performance was studied. Implemented the whole system in veroboard.
4. Digital Fault simulator and PODEM test stimulus generator: Implemented fault simulator and PODEM for test stimulus generation for digital circuit. PODEM and fault simulator was tested in some benchmark circuit.
5. Wide-band down-conversion receiver chain development: A wide-band direct down-conversion receiver (LNA, balun, mixer) was designed in Agilent Advanced Design System environment. It was tested for a family of specification.
6. Study of nonlinear control algorithms*:* Different controlling algorithm for a non-linear system has been implemented in MATLAB and a comparative study has been done of their stability and timing performance.
7. Analog Integrated Circuit Design: A voltage controlled regulated cascode current source has been designed in LTSpice with some target certain specification. The design was able to meet all of the requited specification.

RELEVANT COURSEWORK COMPLETED

Advanced VLSI systems, System in Sub-nanometer Nodes, Fault Tolerant Computing, Digital System Testing, Wireless IC Design, Analog Integrated Circuit Design, Nonlinear Systems, Physical Design Automation, Introduction to Microelectronics Technology.

PUBLICATION

1. **M. I. Momtaz**, S. Banerjee, S. Pandey, J. Abraham, A. Chatterjee "Cross-Layer Control Adaptation for Autonomous System Resilience", IEEE International On-Line Testing Symposium (IOLTS), 2018 [Accepted]
2. **M. I. Momtaz**, S. Banerjee, A. Chatterjee, "On-Line Diagnosis and Compensation for Parametric Failures in Linear State Variable Circuits and Systems Using Time-Domain Checksum Observers", IEEE VLSI Test Symposium (VTS), 2017, pp 1-6
3. **M. I. Momtaz**, S. Banerjee, A. Chatterjee, "Probabilistic Error Detection and Correction in Switched Capacitor Circuits Using Checksum Codes", 23rd IEEE International Symposium on On-Line Testing and Robust System (IOLTS), 2017, pp 271-276
4. **M. I. Momtaz**, S. Banerjee, A. Chatterjee, "Real-Time DC Motor Error Detection and Control Compensation Using Linear Checksums", IEEE VLSI Test Symposium (VTS), 2016, pp 1-6
5. S. Banerjee, **M. I. Momtaz**, A. Chatterjee, "Concurrent Error Detection in Nonlinear Digital Filters Using Checksum Linearization and Residue Prediction", IEEE International On-Line Testing Symposium (IOLTS), 2015, pp 53-58
6. **M. I. Momtaz**, M. M. S. Hassan, "Analytical expression for storage time and injection ratio of a non-uniformly doped n-Si SBD", International Conference on Devices, Circuits and Systems (ICDCS), 2012, pp 610-613
7. M. M. Alam, **M. I. Momtaz**, M. A. Zaman, S. A. Mamun, M. Gaffar, A. Iqbal, M. A. Matin, "Estimation of Electron-Phonon Coupling Constant of Nb and Bi2212 by Modeling the Electron-Lattice Interaction Spectral Function", CUTSE International Conference, 2011, pp 1-3

ACADEMIC HONORS

- Fellowship award, Georgia Institute of Technology, 2014-2015
- Best paper award, 3rd Student Paper Contest, IEEE EDSSC BD Chapter, 2011
- Dean's list award, Department of EEE, BUET, 2004-2009
- University Merit scholarship, Department of EEE, BUET, 2004-2009

LEADERSHIP EXPERIENCES

- Participated in Meindl Legacy "Teachable Moment" program (Feb 2015 – August 2016). Here I played active role to encourage today's K-12 students to impact the future of STEM research. Until now, I have demonstrated simple applications of nanoelectronics to 500 K-12 students.
- Member, Technical committee, 7th International Conference on Electrical and Computer Engineering (ICECE),Dhaka, Bangladesh, Dec 20-22, 2012
- Secretary (2007-09), IEEE BUET Student Branch (SB)-Organized student paper contests, IEEE Day `SPARKS' '07 as well as regular activities like membership drives, plan tours, career development activities, research seminars.

REFEREES of Md Imran Momtaz

1. Dr. Abhijit Chatterjee
   Professor, Georgia Institute of Technology
   Email: abhijit.chatterjee@ece.gatech.edu
2. Estella Silva
   Engineering Manager,
   Texas Instruments Inc.
   Email: Estella.Silva@ti.com
3. Keiichi McGuire
   Analog Verification Engineer
   Texas Instruments Inc.
   Email: Keiichi.McGuire@ti.com